CLAIMS

[00123] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory element comprising:

at least one resistance variable material layer;

at least one metal-containing layer; and

at least one conducting channel formed within said resistance variable material layer, said conducting channel configured to receive and expel metal ions in response to write, erase, and read voltages applied to said memory element.

2. The memory element of claim 1, wherein said resistance variable material layer is a chalcogenide glass layer.

3. The memory element of claim 2, wherein said chalcogenide glass layer has a stoichiometry of Ge_xSe_{100-x}.

4. The memory element of claim 3, wherein said chalcogenide glass layer has a stoichiometry from about $Ge_{18}Se_{82}$ to $Ge_{25}Se_{75}$.

5. The memory element of claim 4, wherein said chalcogenide glass layer is a doped chalcogenide glass layer.

6. The memory element of claim 5, wherein said doped chalcogenide glass layer is doped with metal ions.

7. The memory element of claim 6, wherein said metal ions are silver ions.

8. The memory element of claim 7, wherein said doped chalcogenide glass layer is from about 150 Å to about 600 Å thick.

9. The memory element of claim 8, wherein said doped chalcogenide glass layer has metal-chalcogen regions which are aligned to form said conducting channel.

10. The memory element of claim 9, wherein said metal-chalcogen regions are Ag_2Se regions within a GeSe glass backbone.

11. The memory element of claim 10, wherein said Ag_2Se regions become aligned upon application of a conditioning voltage to the memory element.

12. The memory element of claim 11, wherein said conditioning voltage is greater than subsequent write, read, and erase voltages.

13. The memory element of claim 12, wherein the Ag_2Se regions form at least one conducting channel within the doped chalcogenide glass layer.

14. The memory element of claim 11, wherein prior to application of said conditioning voltage, said memory element has a first resistance state and after application of said conditioning voltage to said memory element, said memory element has a second resistance state lower than said first resistance state.

15. The memory element of claim 14, wherein said write, erase, and read voltages have an absolute magnitude lower than that of said conditioning voltage.

16. The memory element of claim 15, wherein said write voltage produces a third resistance state lower than the second resistance state.

17. The memory element of claim 16, wherein a second write voltage produces a fourth resistance state lower than said third resistance state.

18. The memory element of claim 3, wherein said chalcogenide glass layer has a stoichiometry from about $Ge_{20}Se_{80}$ to $Ge_{43}Se_{57}$.

19. The memory element of claim 18, wherein said chalcogenide glass layer has a stoichiometry of $Ge_{40}Se_{60}$.

20. The memory element of claim 18, wherein said chalcogenide glass layer is from about 150 Å to about 500 Å thick.

21. The memory element of claim 20, wherein the at least one metal-containing layer is formed over said chalcogenide glass layer.

22. The memory element of claim 21, wherein said at least one metal-containing layer is from about 300 Å to about 1200 Å thick.

23. The memory element of claim 1, wherein said at least one metal-containing layer is an Ag_2Se layer.

24. The memory element of claim 1, wherein said resistance variable material has a germanium-selenide glass backbone.

25. The memory element of claim 24, wherein when a conditioning pulse is applied to the memory element, Ag_2Se is driven into said germanium-selenide glass backbone.

26. The memory element of claim 25, wherein said conditioning pulse has a pulse duration of from about 10 to about 500 ns and greater than about 700 mV.

27. The memory element of claim 26, wherein the Ag_2Se is bonded to the germanium-selenide glass backbone forming at least one conducting channel within the chalcogenide glass layer.

28. The memory element of claim 27, further comprising a second metal-containing layer formed over the first metal-containing layer.

29. The memory element of claim 28, wherein said second metal-containing layer comprises silver ions.

30. The memory element of claim 29, wherein the silver ions are driven in and out of the at least one conducting channel by applying different voltages.

31. A memory element comprising:

at least one doped chalcogenide glass layer, said doped chalcogenide glass layer comprising polarized metal-chalcogen regions within a glass backbone, wherein said polarized metal-chalcogen regions form at least one conducting channel for receiving and expelling metal ions within said doped chalcogenide glass layer in response to write, erase, and read voltages applied to said memory element; and

first and second electrodes electrically coupled to said doped chalcogenide glass layer.

32. The memory element of claim 31, wherein said polarized metal-chalcogen regions are silver-selenide regions.

33. The memory element of claim 31, wherein said doped chalcogenide glass layer has a stoichiometry that is from about $Ge_{18}Se_{82}$ to about $Ge_{25}Se_{75}$.

34. The memory element of claim 32, wherein said silver-selenide regions are physically aligned and polarized in response to a conditioning voltage applied to the memory element.

35. The memory element of claim 34, wherein said conditioning voltage changes said memory element from a first resistance state to a second resistance state, said second resistance state being lower than said first resistance state.

36. The memory element of claim 35, wherein said write voltage changes said memory element from a second resistance state to a third resistance state, said third resistance state being lower than said second resistance state.

37. The memory element of claim 36, wherein applying a second write voltage to said memory element moves said memory element from a third resistance state to a fourth resistance state, said fourth resistance state being lower than said third resistance state.

38. The memory element of claim 34, further comprising a metal-containing layer formed over said doped chalcogenide glass layer.

39. The memory element of claim 39, wherein said metal-containing layer is silver.

40. A memory element comprising:

at least one chalcogenide glass layer, said chalcogenide glass layer further comprising bonded regions of metal and glass, wherein said bonded regions of metal and glass form at least one conducting channel within said chalcogenide glass layer;

at least one metal-containing layer formed over said chalcogenide glass layer; and

first and second electrodes electrically coupled to said chalcogenide glass layer.

41. The memory element of claim 40, wherein said chalcogenide glass layer has a stoichiometry that is from about $Ge_{20}Se_{80}$ to about $Ge_{43}Se_{57}$.

42. The memory element of claim 41, wherein said chalcogenide glass layer has a stoichiometry of about $Ge_{40}Se_{60}$.

43. The memory element of claim 40, wherein said chalcogenide glass layer is from about 150 Å to about 500 Å thick.

44. The memory element of claim 40, wherein said at least one metal-containing layer is from about 300 Å to about 1200 Å thick.

45. The memory element of claim 44, wherein said at least one metal-containing layer is an Ag_2Se layer.

46. The memory element of claim 40, wherein said chalcogenide glass has a germanium-selenide glass backbone.

47. The memory element of claim 46, wherein the bonded region of metal is Ag_2Se bonded to germanium-selenide.

48. The memory element of claim 40, wherein said memory element has a first resistance state.

49. The memory element of claim 48, wherein applying a write voltage moves said memory element from said first resistance state to a second resistance state, said second resistance state being lower than said first resistance state.

50. The memory element of claim 49, wherein applying a second write voltage to said memory element moves said memory element from said second resistance state to a third resistance state, said third resistance state being lower than said second resistance state.

51. The memory element of claim 40, further comprising a second metal-containing layer formed over the first metal-containing layer.

52. The memory element of claim 51, wherein said second metal-containing layer comprises silver ions.

53. The memory element of claim 52, wherein the silver ions are driven into and out of the at least one conducting channel by applying different voltages.

54. The memory element of claim 40, further comprising a second chalcogenide glass layer formed over said metal-containing layer.

55. The memory element of claim 54, wherein said second chalcogenide glass layer is from about 100 Å to about 300 Å thick.

56. The memory element of claim 55, further comprising a second metal-containing layer formed over the second chalcogenide glass layer.

57. The memory element of claim 56, wherein said second metal-containing layer is from about 100 Å to about 500 Å thick.

58. The memory element of claim 57, further comprising a third metal-containing layer formed over said second metal-containing layer.

59. The memory element of claim 58, wherein said third metal-containing layer comprises silver ions.

60. The memory element of claim 59, wherein the silver ions are driven into and out of the at least one conducting channel by applying different voltages.

61. A method of forming a memory element, said method comprising:

forming at least one resistance variable material layer;

forming at least one metal-containing layer adjacent said resistance variable material; and

forming at least one conducting channel within said resistance variable material layer by applying a conditioning voltage to the memory element.

62. The method of claim 61, wherein said resistance variable material layer is a chalcogenide glass layer.

63. The method of claim 62, wherein said chalcogenide glass layer has a stoichiometry of Ge_xSe_{100-x}.

64. The method of claim 63, wherein said chalcogenide glass layer has a stoichiometry from about $Ge_{18}Se_{82}$ to $Ge_{25}Se_{75}$.

65. The method of claim 64, wherein said chalcogenide glass layer is doped with metal ions.

66. The method of claim 65, wherein said metal ions are silver ions.

67. The method of claim 66, wherein said doped chalcogenide glass layer is from about 150 Å to about 600 Å thick.

68. The method of claim 67, wherein said doped chalcogenide glass layer has polarizable metal-chalcogen regions.

69. The method of claim 68, wherein said polarizable metal-chalcogen regions are Ag_2Se regions within a germanium-selenide glass backbone.

70. The method of claim 69, wherein said Ag_2Se regions become aligned upon application of said conditioning voltage to said memory element.

71. The method of claim 70, wherein said conditioning voltage is greater than subsequent write, read, and erase voltages.

72. The method of claim 70, wherein the Ag_2Se regions form at least one conducting channel by becoming polarized and aligning within the doped chalcogenide glass layer.

73. The method of claim 61, wherein prior to applying said conditioning voltage, said memory element has a first resistance state and after applying said conditioning voltage to said memory element, said memory element has a second resistance state lower than said first resistance state.

74. The method of claim 73, wherein subsequent write, read, and erase voltages have an absolute magnitude lower than that of said conditioning voltage.

75. The method of claim 74, wherein applying a write voltage produces a third resistance state lower than the second resistance state.

76. The method of claim 75, wherein applying a second write voltage produces a fourth resistance state lower than said third resistance state.

77. The method of claim 61, wherein said chalcogenide glass layer has a stoichiometry from about $Ge_{20}Se_{80}$ to $Ge_{43}Se_{57}$.

78. The method of claim 77, wherein said chalcogenide glass layer has a stoichiometry of $Ge_{40}Se_{60}$.

79. The method of claim 77, wherein said chalcogenide glass layer is from about 150 Å to about 500 Å thick.

80. The method of claim 61, wherein said at least one metal-containing layer is from about 300 Å to about 1200 Å thick.

81. The method of claim 80, wherein said at least one metal-containing layer is an Ag_2Se layer.

82. The method of claim 81, wherein the conditioning voltage is applied to the memory element driving Ag_2Se into the chalcogenide glass layer.

83. The method of claim 82, wherein said conditioning voltage has a pulse duration of from about 10 to about 500 ns and greater than about 700 mV.

84. The method of claim 83, wherein the chalcogenide glass layer has a germanium-selenide glass backbone.

85. The method of claim 84, wherein the Ag_2Se bonds to the germanium-selenide glass backbone forming at least one conducting channel within said chalcogenide glass layer.

86. The method of claim 80, further comprising forming a second metal-containing layer over the first metal-containing layer.

87. The method of claim 86, wherein said second metal-containing layer comprises silver ions.

88. The method of claim 87, wherein said silver ions are driven into and out of the at least one conducting channel by applying different voltages.

89. A method of forming a memory element, said method comprising:

forming at least one doped chalcogenide glass layer with polarizable metal-chalcogen regions within a glass backbone;

electrically coupling first and second electrodes to said doped chalcogenide glass layer; and

polarizing said metal-chalcogen regions with a conditioning voltage applied to said electrodes to form at least one conducting channel comprising said polarized metal-chalcogen regions, said conducting channel configured to receive and expel metal ions in response to write, erase and read voltages applied to said memory element.

90. The method of claim 89, wherein said polarizable metal-chalcogen regions are silver-selenide regions.

91. The method of claim 89, wherein said doped chalcogenide glass layer has a stoichiometry that is from about $Ge_{18}Se_{82}$ to about $Ge_{25}Se_{75}$.

92. The method of claim 90, wherein said polarizable silver-selenide regions align to form at least one conducting channel after the conditioning voltage is applied.

93. The method of claim 89, wherein said conditioning voltage changes said memory element from a first resistance state to a second resistance state, said second resistance state being lower than said first resistance state.

94. The method of claim 93, wherein applying a write voltage changes said memory element from a second resistance state to a third resistance state, said third resistance state being lower than said second resistance state.

95. The method of claim 94, wherein applying a second write voltage to said memory element moves said memory element from a third resistance state to a fourth resistance state, said fourth resistance state being lower than said third resistance state.

96. The method of claim 89, further comprising forming a metal-containing layer over said doped chalcogenide glass layer.

97. The method of claim 96, wherein said metal-containing layer comprises silver.

98. The method of claim 97, wherein said metal-containing layer provides metal ions that move in and out of the conducting channel.

99. A method of forming a memory element, said method comprising:

forming at least one chalcogenide glass layer;

forming at least one metal-containing layer over said chalcogenide glass layer;

electrically coupling first and second electrodes to said chalcogenide glass layer; and

applying a conditioning pulse to the memory element to bond regions of metal and glass within said chalcogenide glass layer, said bonded regions forming at least one conducting channel within said chalcogenide glass layer.

100. The method of claim 99, wherein said chalcogenide glass layer has a stoichiometry that is from about $Ge_{20}Se_{80}$ to about $Ge_{43}Se_{57}$.

101. The method of claim 100, wherein said chalcogenide glass layer has a stoichiometry that is $Ge_{40}Se_{60}$.

102. The method of claim 100, wherein said chalcogenide glass layer is from about 150 Å to about 500 Å thick.

103. The method of claim 99, wherein said at least one metal-containing layer is from about 300 Å to about 1200 Å thick.

104. The method of claim 103, wherein said at least one metal-containing layer is an Ag_2Se layer.

105. The method of claim 102, wherein said chalcogenide glass has a germanium-selenide glass backbone.

106. The method of claim 105, wherein the bonded regions of metal is Ag_2Se bonded to germanium-selenide.

107. The method of claim 99, wherein the memory element has a first resistance state.

108. The method of claim 107, wherein applying a write voltage moves said memory element from said first resistance state to a second resistance state, said second resistance state being lower than said first resistance state.

109. The memory element of claim 108, wherein applying a second write voltage to said memory element moves said memory element from said second resistance state to a third resistance state, said third resistance state being lower than said second resistance state.

110. The method of claim 99, further comprising forming a second metal-containing layer over the first metal-containing layer.

111. The method of claim 110, wherein said second metal-containing layer comprises silver ions.

112. The method of claim 111, wherein said silver ions are driven into and out of the at least one conducting channel by applying a write, erase or read voltage.

113. The method of claim 99, further comprising forming a second chalcogenide glass layer over said at least one metal-containing layer.

114. The method of claim 113, wherein said second chalcogenide glass layer is from about 100 Å to about 300 Å thick.

115. The method of claim 114, further comprising forming a second metal-containing layer over said second chalcogenide glass layer.

116. The method of claim 115, wherein said second metal-containing layer is from about 100 Å to about 500 Å thick.

117. The method of claim 116, further comprising forming a third metal-containing layer over said second metal-containing layer.

118. The method of claim 117, wherein said third metal-containing layer comprises silver ions.

119. The method of claim 118, wherein said silver ions are driven into and out of the at least one conducting channel by applying a write, erase, or read voltage.

120. A method of operating a memory element comprising a conducting at least one conducting channel formed within a chalcogenide glass material, said method comprising:

applying a conditioning voltage to physically align metal-chalcogen regions which form said at least one conducting channel within a chalcogenide glass material, said first voltage moving the memory element from a first to a second resistance state, said first resistance state exhibiting a higher resistance than said second resistance state; and

applying a first write voltage to move metal ions into said conducting channel and placing the memory element in a third resistance state, said third resistance state being lower than said second resistance state.

121. The method of claim 120, further comprising applying a second write voltage to move the memory element into a fourth resistance state, said fourth resistance state being equal to or lower than said third resistance state.

122. The method of claim 121, further comprising applying an erase voltage to move the memory element into a fifth resistance state, said fifth resistance state being higher than said second and third resistance state.

123. The method of claim 120, wherein said first resistance state is approximately 1 GΩ.

124. The method of claim 120, wherein said second resistance state is approximately 1 MΩ.

125. The method of claim 120, wherein said third resistance state is approximately 10kΩ.

126. The method of claim 121, wherein said fourth resistance state is less than 10kΩ.

127. The method of claim 120, wherein the write voltage is less than the conditioning voltage in absolute amplitude.

128. The method of claim 121, wherein the second write voltage is less than or equal to the first write voltage in absolute amplitude.

129. The method of claim 122, wherein the erase voltage is applied with inverse polarity compared to the write voltage.

130. A method of operating a memory element comprising a chalcogenide glass material with at least one conducting channel formed from bonded metal and glass regions, said method comprising:

applying a conditioning voltage to condition the memory element, said first voltage moving the memory element from a first resistance state into a second resistance state, wherein said second resistance state is less than said first resistance state; and

applying a write voltage to move the memory element into a third resistance state, said third resistance state being less than said second resistance state.

131. The method of claim 130, further comprising applying a second write voltage to move the memory element into a fourth resistance state; said fourth resistance state being less than said second resistance state.

132. The method of claim 131, further comprising applying an erase voltage to move the memory element into said second resistance state; said second resistance state being higher than said third and fourth resistance states.

133. The method of claim 130, wherein said first resistance state is approximately 1 GΩ.

134. The method of claim 130, wherein said second resistance state is approximately 1 MΩ.

135. The method of claim 130, wherein said third resistance state is approximately 10kΩ.

136. The method of claim 131, wherein said fourth resistance state is approximately less than 10kΩ.

137. The method of claim 130, wherein the write voltage is less than the conditioning voltage in absolute amplitude.

138. The method of claim 131, wherein the second write voltage is less than conditioning voltage in absolute amplitude.

139. The method of claim 132, wherein the erase voltage is applied in inverse polarity from said write voltage.

140. A chalcogenide memory element comprising:

a first electrode;

a doped chalcogenide glass layer formed adjacent to said first electrode comprising polarized Ag_2Se regions within a germanium-selenide glass backbone, said polarized Ag_2Se regions are oriented to form at least one conducting channel for receiving and expelling silver metal ions within said doped chalcogenide glass layer in response to write, erase, and read voltages applied to said chalcogenide memory element;

a silver comprising layer formed adjacent to said doped chalcogenide glass layer, said silver comprising layer providing silver metal ions which flow in and out of the at least conducting channel; and

a second electrode formed adjacent to said silver comprising layer.

141. A chalcogenide memory element comprising:

a first electrode;

a chalcogenide glass layer, said glass layer having a germanium-selenide glass backbone bonded to Ag_2Se regions, wherein said bonded regions form at least one conducting channel within said glass layer;

an Ag_2Se layer formed over said glass layer;

a silver-comprising layer formed over said Ag_2Se layer, said silver-comprising layer containing silver metal ions which move in and out of said conducting channel in response to different bias voltages; and

a second electrode.

142. A chalcogenide memory element comprising:

a first electrode;

a first chalcogenide glass layer, said first glass layer having a germanium-selenide glass backbone bonded to Ag_2Se regions, wherein said bonded regions form at least one conducting channel within said first glass layer;

an Ag_2Se layer formed over said first glass layer;

a second chalcogenide glass layer formed over said Ag_2Se layer;

a silver-comprising layer formed over said second glass layer, said silver-comprising layer containing silver metal ions which move in and out of said conducting channel in response to different bias voltages; and

a second electrode.

143. A chalcogenide memory element comprising:

a first electrode;

a first chalcogenide glass layer, said first glass layer having a germanium-selenide glass backbone bonded to Ag_2Se regions, wherein said bonded regions form at least one conducting channel within said first glass layer;

a first Ag_2Se layer formed over said first glass layer;

a second chalcogenide glass layer formed over said Ag_2Se layer;

a second Ag_2Se layer formed over said second glass layer;

a silver-comprising layer formed over said second Ag_2Se layer, said silver-comprising layer containing silver metal ions which move in and out of said conducting channel in response to different bias voltages; and

a second electrode.